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(54) **Semiconductor device and liquid crystal display.**

(57) A semiconductor device has an NMOS transistor and a PMOS transistor formed on at least one monocrystal Si region formed in a thin-film Si layer formed on an insulation layer. The thickness T_{BOX} of the insulation layer on which the NMOS and PMOS transistors are formed, the voltage V_{SS} of a low-voltage power supply and the voltage V_{DD} of a high-voltage power supply for the NMOS and PMOS transistors satisfy a relationship expressed by the following equation :
$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$
where $K_1 \equiv \varepsilon_{BOX}(Q_{BN} + Q_{BP})$, $K_2 \equiv 2\phi_{FN} + 2\phi_{FP} - 1.03$, ε_{BOX} is the dielectric constant of the base insulation layer, Q_{BN} and Q_{BP} are bulk charges when the widths of depletion layers of the NMOS and PMOS transistors are maximized, and ϕ_{FN} and ϕ_{FP} are pseudo Fermi potentials of the NMOS and PMOS transistors.

FIG. 1(a)
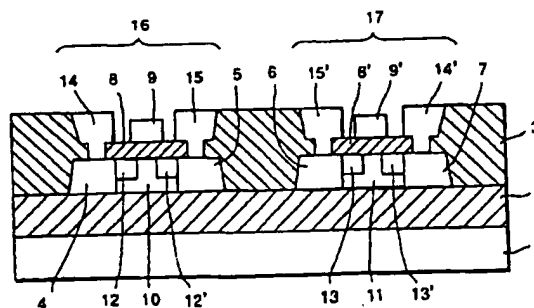
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BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor device having a P-channel metal oxide silicon (PMOS) transistor and an N-channel metal oxide silicon (NMOS) transistor and to a liquid crystal display using the semiconductor device as a peripheral drive circuit and the PMOS transistor as a pixel electrode switching device.

Description of the Related Art

With the recent rapid progress of semiconductor technology, there has been a demand for smaller, high-speed and small-power-consumption semiconductor devices and apparatuses using such devices. The development of complementary MOS (CMOS) inverters using P-channel and N-channel enhancement type MOS field effect transistors (FET) as load and inverter devices among such apparatuses is being further promoted because the power consumption of this type of inverter is very small, although a complicated manufacturing process is required.

Fig. 1(a) shows an example of a CMOS inverter in section. A transistor 16 is an NMOS transistor while a transistor 17 is a PMOS transistor. The transistors 16 and 17 are formed on a substrate while being insulated by a base insulation layer 2 and separated from each other by SiO_2 3. The MOS transistor 16 is constituted of an N^+ drain 5, a P-channel region 10, an N-type field limiting regions 12, 12', a gate insulation film 8, a gate electrode 9, a source electrode 14, and a drain electrode 15. The gate electrode is ordinarily formed of a polycrystalline Si, and the source and drain electrodes are formed of Al.

The PMOS transistor 17 is constituted of a P^+ drain 6, a P^+ source 7, N-channel region 11, a P-type field limiting regions 13, 13', a gate insulation film 8', a gate electrode 9', a source electrode 14', and a drain electrode 15'.

Fig. 1(b) is an equivalent circuit diagram of the above-described CMOS inverter. As illustrated, the drain electrode 15 of the NMOS transistor 16 and the drain electrode 15' of the PMOS transistor 17 are connected to a common output electrode. An output voltage at this output electrode is represented by V_{out}. The source electrode 14 of the NMOS transistor 16 is connected to a low-voltage power supply, while the source electrode 14' of the PMOS transistor 17 is connect d t a high-voltage power supply. The voltage of these power supplies are r presented by V_{SS} and V_{DD}. The substrat 1 forms gate electrodes of parasitic MOS transistors with respect to the NMOS transistor 16 and the PMOS transistor 17. That is, a parasitic PMOS transistor having a gate insulation layer corresponding to the base insulation layer 2, a

channel r gion corresponding to the region 11, and a source and a drain corresponding to th drain 6 and the source 7 is formed, whil a parasitic NMOS transistor having a gate insulation layer corresponding to the base insulation layer 2, a channel region corresponding to the region 10, and a source and a drain corresponding to the source 4 and the drain 5 is formed. V_{back} in Fig. 1(b) represents a voltage input to these parasitic CMOS transistors.

Fig. 9 shows input-output characteristics of a conventional CMOS inverter. In the case of conventional CMOS inverters, it is difficult to increase the absolute value of threshold voltages of parasitic MOS transistors. If the threshold values of the parasitic NMOS and PMOS transistors are V_{thbn}, and Vthbp, respectively, $V_{thbn} - V_{thbp}$ (the threshold value of the PMOS transistor being ordinarily negative) > $V_{DD} - V_{SS}$, that is, $V_{SS} < V_{SS} + V_{thbn} < v_{DD} + V_{thbp} < V_{DD}$. With respect to any value of V_{back}, the parasitic NMOS or PMOS transistor can operate. As shown in Fig. 9, in the case where V_{in} becomes closer to V_{DD} when V_{back} is about zero, the parasitic PMOS transistor is operating and a leak current through the PMOS transistor inhibits the output from completely dropping to V_{SS}. On the other hand, in the case where V_{in} becomes closer to V_{SS} when V_{back} is about 3 V, the parasitic NMOS transistor is operating and a leak current through the NMOS transistor inhibits the output from completely rising to V_{DD}.

As described above, a leak current flows by the operation of a parasitic CMOS transistor in the conventional CMOS inverter, resulting in failure to obtain an ideal input-output characteristic of the transistor.

For manufacture of a semiconductor device, monocrystal Si having a high carrier mobility is desirable in terms of high-speed driving performance. Conventionally, a SIMOX (separation by implanted oxygen) method has been used to form a monocrystal Si layer on an insulation layer. The thickness of the base insulation layer attained by this method is at most 5,000 Å. To increase the absolute value of the threshold value, it is necessary to increase the thickness of the base insulation layer according to a relationship between the base insulation layer thickness and the threshold value described later. However, it has been impossible to increase the base insulation layer thickness to a value greater than 5,000 Å for this manufacturing problem.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device free from the abov -described problem and a liquid crystal display using the semiconductor device.

Another object of the present invention is to provid a s miconductor device having an insulation layer thick enough to solve the above-described prob-

lem and a monocrystal silicon thin film formed on the insulation layer, and a liquid crystal display using the semiconductor device.

To achi ve thes obj cts, according to the pres- nt invention, there are provided a semiconductor de- vice and a liquid crystal display using the semicon- ductor device in a peripheral drive circuit, the semi- conductor device comprising an NMOS transistor and a PMOS transistor formed on at least one monocrys- tal Si region formed in a thin-film Si layer formed on an insulation layer, wherein the thickness T_{BOX} of the insulation layer on which the NMOS and PMOS tran- sistors are formed, the voltage V_{SS} of a low-voltage power supply and the voltage V_{DD} of a high-voltage power supply for the NMOS and PMOS transistors satisfy a relationship expressed by the following equation:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

where $K_1 \equiv \varepsilon_{BOX} (Q_{BN} + Q_{BP})$, $K_2 \equiv 2\phi_{FN} + 2\phi_{FP} - 1.03$, ε_{BOX} is a dielectric constant of the base insulation lay- er, Q_{BN} and Q_{BP} are bulk charges when the widths of depletion layers of the NMOS and PMOS transistors are maximized, and ϕ_{FN} and ϕ_{FP} are pseudo Fermi po- tentials of the NMOS and PMOS transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a) is a cross-sectional view of an example of a semiconductor device in accordance with the present invention;

Fig. 1(b) is a equivalent circuit diagram of the semiconductor device shown in Fig. 1;

Fig. 2 is a diagram of an input-output character- istic of a CMOS inverter in accordance with a first embodiment of the present invention;

Fig. 3 is a diagram of film thickness-threshold value characteristics of a parasitic NMOS transis- tor;

Fig. 4 is a diagram of film thickness-threshold value characteristics of a parasitic PMOS transis- tor;

Fig. 5 is a diagram of a relationship between the threshold value and the film thickness of the parasitic MOS transistors;

Fig. 6(a) is a diagram of a SIMOX process prac- ticed in accordance with a fourth embodiment of the present invention;

Fig. 6(b) is a oxygen concentration profile of the process of the fourth embodiment;

Fig. 7 is an illustration of a fifth embodiment of the present invention;

Fig. 8 is a cross-sectional view of a sixth embodi- m nt of the present invention; and

Fig. 9 is a diagram of input-output characteristics of a conventional CMOS inverter.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described below in detail.

As described above, in accordance with the prin- ciple of the operation of a CMOS inverter, a condition necessary for the existence of a value of V_{back} with which parasitic NMOS and PMOS transistors cannot operate is $V_{SS} + V_{thbn} < V_{DD} + V_{thbp}$.

V_{thbn} and V_{thbp} can be expressed as shown below.

$$V_{thbn} = + (Q_{BN}/C_{BOX}) + 2\phi_{FN} + V_{FB}$$
$$Q_{BN} = \sqrt{2q\varepsilon N_{CN}(2\phi_{FN})}$$
$$V_{FB} = - qQ_{SS}/C_{BOX} - 0.88$$
$$V_{thbp} = - (Q_{BP}/C_{BOX}) - 2\phi_{FP} + V_{FB}$$
$$Q_{BP} = \sqrt{2q\varepsilon N_{CP}(2\phi_{FP})}$$
$$V_{thbp} = - qQ_{SS}/C_{BOX} + 0.15$$

C_{BOX}: the capacity per unit area of the base in- sulation layer (F/cm^2)

q: elementary electric charge

N_C: a channel impurity concentration

ϕ_{FN}, ϕ_{FP}: psuedo Fermi potentials of the NMOS and PMOS transistors

$\phi F: = (kT/q)1n(N_c/n_i)$

k: Boltzmann's constant

T: absolute temperature

n_i: an intrinsic carrier density of Si

V_{FB}: a flat band voltage

Therefore,

$$V_{thbn} - V_{thbp} = (Q_{BN} + Q_{BP}/C_{BOX}) + 2\phi_{FN} + 2\phi_{FP} - 1.03.$$

Each of the Q_{BN}, Q_{BP}, ϕ_{FN}, and ϕ_{FP} in the above has only one value if the impurity concentrations N_{cn} and N_{cp} are determined.

Since $C_{BOX} = \varepsilon_{BOX}/T_{BOX}$

ε_{BOX}: a dielectric constant of the base insula- tion layer

T_{BOX}: the thickness of the base insulation lay- er,

only C_{BOX} in the above equation is changed with the thickness of the base insulation layer. Accordingly,

$$V_{thbn} - V_{thbp} = K_1 T_{BOX} + K_2$$
where $K_1 \equiv \varepsilon_{BOX} (Q_{BN} + Q_{BP})$ and
$$K_2 \equiv 2\phi_{FN} + 2\phi_{FP} - 1.03.$$
$$\therefore V_{DD} - V_{SS} < V_{thbn} - V_{thbp} = K_1 T_{BOX} + K_2$$
$$\therefore T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

If the base insulation layer has a thickness such as to satisfy this equation, the absolute value of the threshold values can be increased so that occur- rence of a leak current is prevented.

According to the present invention, the method of manufacturing the base insulation layer is not partic- ularly limited so long as the thickness in accordance with the above-described quation is attained. How- ever, the thickness of an insulation layer in the con- venti nal SIMOX ubstrate cannot be indefinitely in- creased, as described above. In accordance with the

present invention, a monocrystal Si region can be formed on a thick insulation layer, for example, by pi-taxial growth on an SIMOX or porous Si substrative member changed in condition, or by laser-ann aling a polycrystalline or amorphous Si thin film.

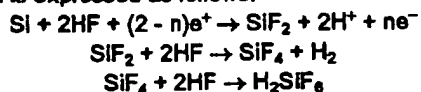The present invention will be described with re-spect to examples thereof.

Embodiment 1

A monocrystal Si thin film was formed by using a porous Si substrate member. A method of manufac-turing this monocrystal Si thin film will be described below.

In the porous Si substrate member used, holes having a diameter of about 600 Å on an average are formed, which were observed through a transmission microscope. The density of the porous Si substrate is at most half that of monocrystal Si, but its monocrys-tal properties are maintained and a monocrystal Si layer can be formed on the porous layer by epitaxial growth. However, a rearrangement of internal holes takes place at 1,000°C or higher, and the character-istics of enhanced etching are thereby impaired. For this reason, a low-temperature growing method, such as a molecular beam epitaxial growth method, a plas-ma chemical vapor deposition (CVD) method, a ther-mal CVD method, a photo-CVD method, a bias sput-tering method, or a liquid crystal growth method, is preferred as a method for growing the Si layer.
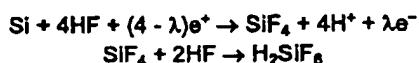
A method in which P-type Si is made porous and a monocrystal layer is thereafter grown by epitaxial growth will be described below.

First, a Si monocrystal substrate member is pre-pared and is processed by an anodization method us-ing a HF solution to form a porous layer therein. While the density of monocrystal Si is 2.33 g/cm³, the den-sity of the porous Si can be changed in the range of 0.6 to 1.1 g/cm³ by changing the HF solution concen-tration in the range of 20 to 50 % by weight. This por-ous layer can easily be formed into a P-type Si sub-strate member for a reason described below.

Porous Si was found in a process of studying electrolytic polishing of a semiconductor. In a dissolu-tion reaction of Si in anodization, positive holes are re-quired for anodization of Si in the HF solution. This re-action is expressed as follows.

$$Si + 2HF + (2 - n)e^+ \rightarrow SiF_2 + 2H^+ + ne^-$$
$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$
$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4 - \lambda)e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$
$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

Symbols e^+ and e^- repres nt hol s and el ctrons, resp ctively. Each of n and λ represents the number of h les, in the relevant quati n, n cessary for dis-solving one Si atom. Porous Si is formed on condition that $n > 2$ or $\lambda > 4$.

From this fact, it can b said that P-type Si in which holes exist can easily b made porous.

On the other hand, it has b n report d that high-d nsity N-type Si can be made porous. Thus, a Si substrate member can be made porous irrespective of being P- or N-type.

Also, the density of the porous layer is a half or less of the original density, since many gaps are formed in the porous layer. Therefore the surface area is greatly increased relative to the volume. The chemical etching speed is thereby increased remark-ably in comparison with the etching speed of the or-dinary monocrystal layer.

Conditions for making monocrystal Si porous by anodization are shown below. A starting material of porous Si formed by anodization is not limited to monocrystal Si, and Si in other crystalline structures can be used.

Applied voltage: 2 (V)
Current density: 30 (mA·cm⁻²)
anodization solution: HF : H_2O : C_2H_5OH = 1 : 1 : 1

Time: 2.4 (hours)
Thickness of porous Si: 300 (µm)
Porosity: 56 %

Si is grown by epitaxial growth on porous Si formed in this manner, thereby forming a monocrys-tal Si thin film. The thickness of the monocrystal Si thin film is, preferably, 50 µm or less, more preferably, 20 µm or less.

A surface of the monocrystal Si thin film is then oxidized. A substrate member which is to finally form a main substrate is prepared and is attached to the oxide film in the monocrystal Si surface. Alternative-ly, a surface of monocrystal Si substrate member newly prepared is oxidized and is attached to the monocrystal Si layer on the porous Si substrate mem-ber. The reason for the provision of such an oxide film between the substrate member and the monocrystal Si layer is because an interface level generated from a base interface of a Si active layer with an oxide film can be smaller than, for example, an interface level from a base interface with a glass provided as a sub-strate member. It is possible to greatly improve char-acteristics of an electronic device by forming such an oxide film interface. Further, only a monocrystal Si thin film prepared by removing a porous Si substrate member by a selective etching process described lat-er may be attached to a new substrate member. Two substrate members can be attached closely enough to prevent separation between them by the van der Waals force, if their surfaces are washed and there-after brought into contact with each other at room t mperature. However, th substrate members in this state are processed by a heat treatment in a nitrogen atmosphere at a temperature in the range of 200 to 900°C, preferably, 600 to 900°C.

An Si_3N_4 lay r is formed as an tching prevention

film by deposition over the ntire surface of the two attach d substrate members. Only th portion of the Si₃N₄ layer on th surface of th porous Si substrate member is then removed. Apiezon wax may be used instead of Si₃N₄. Thereafter, the porous Si substrate member is entirely removed by etching or other means. A semiconductor substrate having a thin monocrystal Si layer can be obtained in this manner.

A selective etching method for etching only the porous Si substrate member by non-electrolyte wet etching will be described below.

As an etching liquid having no etching effect with respect to crystalline Si but capable of selectively tching only porous Si, it is preferable to use hydrofluoric acid, buffered hydrofluoric acid of ammonium fluoride (NH₄F), hydrogen fluoride (HF) or the like, a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid and hydrogen peroxide solution, a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid and alcohol, or a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid, hydrogen peroxide solution and alcohol. The substrate members attached to each other undergo etching by being wetted with such an etching liquid. The etching speed depends upon the concentration of hydrofluoric acid, buffered hydrofluoric acid and hydrogen peroxide in the solution and upon the temperature. By the addition of the hydrogen peroxide solution, the oxidation of Si is promoted and the reaction speed is increased in comparison with an etching liquid to which no hydrogen peroxide solution is added. Further, the reaction speed can be controlled by changing the proportion of the hydrogen peroxide solution. By the addition of alcohol, bubbles of a reaction product gas can be instantly removed from the etched surface without agitation, and the porous Si can be etched uniformly and efficiently.

The HF concentration in buffered hydrofluoric acid is set in the range of, preferably, 1 to 95 %, more preferably, 1 to 85 %, and further preferably, 1 to 70 % by weight of the etching liquid.

The NH₄F concentration in buffered hydrofluoric acid is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 5 to 80 % by weight of the etching liquid.

The HF concentration is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 5 to 80 % by weight of the etching liquid.

The H₂O₂ concentration is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 10 to 80 % by weight of the etching liquid, and is s t in a rang such that the above-described eff ct of hydrogen peroxide solution can be attained.

The alcohol concentration is set in the range of, preferably, 80 % r less, more preferably, 60 % or less, and further preferably, 40 % or l ss by weight of

the tching liquid, and is set in a range such that the above-described eff ct of alcohol can b attain d.

The temp rature is set in the rang of, preferably, 0 to 100°C, mor preferably, 5 to 80°C, and further preferably, 5 to 60°C.

Alcohol used in accordance with the present invention comprises ethyl alcohol, isopropyl alcohol and the like, i.e., alcohols which entail no considerable problem in the manufacturing process in practice and which ensure the above-described alcohol addition effect.

In the semiconductor substrate obtained in this manner, a thin large-area layer of monocrystal Si equivalent to the ordinary Si wafer is formed flat and uniformly to cover the entire area on the substrate.

A monocrystal Si thin film, such as the one described in detail in the specification of European Patent Laid-Open Publication No.469830, can be specifically used as the above-described monocrystal Si thin film in accordance with the present invention.

In this embodiment of the invention, a SiO₂ film having a thickness of 10,000 Å was formed on a monocrystal Si substrate, and was attached to a monocrystal Si thin film to form a base insulation layer. A CMOS inverter such as that shown in Fig. 1 was manufactured by using this base insulation layer. The method of setting the above-mentioned film thickness will be described below.

Fig. 3 shows film thickness (T_{BOX})-threshold value V_{thbn}) characteristics of a parasitic NMOS transistor with Q_{ss} (fixed positive charge on the base insulation layer) (cm^{-2}) used as a parameter. The density in the channel region was set to 1×10^{16} cm^{-3}.

Fig. 4 shows film thickness-threshold value (V_{thbp}) characteristics of a parasitic PMOS transistor with Q_{ss} used as a parameter. The density in the channel region was set to 5×10^{16} cm^{-3}.

Fig. 5 shows a relationship between the film thickness and the threshold value difference V_{thbn} - V_{thbp} between the two transistors on the basis of the data shown in Figs. 3 and 4 with respect to the channel densities of 1×10^{16} cm^{-3} and 5×10^{16} cm^{-3}.

As described above, for the existence of a value of V_{back} with which the parasitic NMOS and PMOS transistors cannot operate, at least $V_{DD} - V_{SS} < V_{thbn}$ - V_{thbp} must be satisfied. The graph of Fig. 5 is formed by using, as a parameter, allowable values of currents flowing in gate voltage ranges below the threshold values. In Fig. 1, the relationship between V_{thbn} - V_{thbp} and T_{BOX} is shown with respect to a current of 1 μm flowing when $V_{back} = V_{thbn}$, V_{thbp}, a current down by a factor of 10^2 therefrom (allowable current = 10 μA), a current d wn by a factor f 10^4 (allowable current = 10 nA), and a current down by a factor of 10^6 (allowable current = 100 pA). There is no influence of Q_{ss} upon the relationship shown in this graph.

In this embodiment, a base insulation lay r thickness T_{BOX} = 10,000 Å was determined from Fig. 5 un-

der conditions: $V_{DD} - V_{SS} = 14$ V, an allowabl current of 100 pA, and a margin of 5 V between the threshold value difference and $V_{DD} - V_{SS}$.

Fig. 2 shows an input-output characteristic of this CMOS inverter. Input-output values closer to an ideal characteristic were exhibited with respect to $V_{DD} = 8$ V, $V_{SS} = -6$ V, and $V_{back} = 3$ V. This CMOS inverter can be used in a driving circuit having a high power supply voltage, 14 V.

Embodiment 2

A semiconductor device was manufactured in the same manner as Embodiment 1 except that a base insulation layer was formed so as to have a three-layer structure formed of 8,000 Å thick layer of SiO_2, a 500 Å thick layer of SiN, and a 1,000 Å thick layer of SiO_2. The thickness of this three-layer film corresponds to about 9,250 Å in terms of the thickness of the SiO_2 single layer structure as determined by conversion with respect to the dielectric constant. In this embodiment, SiN was deposited by a low pressure CVD method. Alternatively, SiN may be formed by being nitrized by rapid thermal annealing at 1,000°C after SiO_2 deposition.

In a case where there is a need to partially remove the Si substrate by etching on the back side thereof, for example, for the purpose of forming a transparent portion such as that of a display portion of a liquid crystal display, etching can easily be stopped since the SiN layer acts as a suitable stopper, and cutting-out can be performed by uniform back-side etching.

The operation at $V_{DD} - V_{SS} = 14$ V was substantially possible, although the threshold values of the parasitic MOS transistors were slightly reduced in comparison with Embodiment 1.

Embodiment 3

Conventionally, a SIMOX substrate is manufactured by a method of injecting, ordinarily, 3 to 5 separated shots of an amount of oxygen ions of 4×10^{17} to 2.4×10^{18} cm^{-2} with acceleration energy of 150 to 300 keV, and thereafter performing a heat treatment at 1,100 to 1,250°C for 2 to 20 hours.

In this embodiment, oxygen ions were injected by double-charging using a charge twice as large as the ordinary charge, while an average ion injection range (ion injection depth) Rp = 8,000 Å and a dispersion of ion injection range ΔRp = 4,000 Å were set. SiO_2 film having a thickness of 10,000 Å was thereby formed. A CMOS inverter similar to that in accordance with Embodiment 1 was manufactured by using this SIMOX substrate. The CMOS inverter obtained had n leak and had an improved characteristic.

Embodiment 4

A SIMOX substrate was manufactured by changing energy for oxygen ion injection by three steps as shown in Fig. 6(a). That is, oxygen ions w re injected under conditions: $R_P = 150$, 250, 400 keV, and ion injection dose = 5×10^{17}, 2×10^{18}, 4×10^{18} cm^{-2}, followed by a heat treatment at 1,200 °C for 36 hours. With an oxygen profile such as that shown in Fig. 6(b), SOI (silicon on insulator) on SiO_2 film having a thickness of about 1.3 μm was realized. A 20 V driving circuit can be made by forming a CMOS inverter on this SIMOX substrate.

Embodiment 5

An active matrix type of liquid crystal display having a semiconductor device in accordance with the present invention was manufactured by forming a polycrystalline or amorphous Si layer on a transparent substrate and by processing a necessary portion thereof by laser annealing so that the processed portion is changed into a monocrystal. Fig. 7(a) is a plan view of this display. A display portion 72 is formed at the center of the substrate and is surrounded by a drive circuit portion 71. Chips integrated in an active matrix and a circuit for driving the matrix are provided on a device region 74 formed in an amorphous region 73. A laser light source used for laser annealing is of a high output (5 to 1,000 mW) type using a helium neon lamp as a light source. In the display in accordance with this embodiment, only the drive circuit is required to have a high-speed switching operation. Therefore, only the drive circuit portion is scanned with the laser light source, as illustrated. The scanned portion is changed into a monocrystal region where the carrier mobility is the same as that in ordinary monocrystal Si, thereby enabling high-speed driving. The manufacturing cost is increased by the laser annealing process. However, the increase in the manufacturing cost is limited by setting a necessary minimum processed region as described above. It is thereby possible to manufacture a high-integration high-resolution liquid crystal display having two hundred thousand or more pixels.

Example 6

Fig. 8 shows an example of a preferred form of the liquid crystal display in accordance with the present invention. In this embodiment, a drive circuit portion 71 is formed on a thick SiO_2 film 83 (having a thickn ss of 10,000 Å, for example), enabling driving of $V_{DD} - V_{SS} = 14$ V. A display portion 72 in which transistors serving as switching devices for applying voltages to liquid crystal cells are arranged in th form of a matrix is formed on a thin SiO_2 film 82. A monocrystal Si substrate 81 at the back sid of the display

portion 72 is partially removed by w t etching, and a space thereby formed is filled with a back packing (silicon rubber) 84 for r inforcem nt This packing is almost transparent and all ws back light from under to pass in order to efficiently illuminate the display portion.

Only PMOS transistors are used as switching devices in the display portion. The back packing 84 has an insulating property. Therefore, even if there are movable ions (ordinarily, positive ions) in the back packing, the parasitic PMOS transistor does not operate by this charge.

Thus, an unnecessary increase in the SiO_2 film is limited to reduce stresses remaining in the SiO_2 film and the device region after cutting-out of the monocrystal silicon substrate. It is thereby possible to avoid an arrangement of liquid crystal cells on the outer device region and to improve image qualities.

As described above, in the semiconductor device in accordance with the present invention, a leak current, relating to the problem of the conventional art, can be prevented by controlling the film thickness of the base insulation layer. The semiconductor device can there perform high speed driving with a high power supply voltage The liquid crystal display of the present invention using the semiconductor device in a drive circuit can be designed for high-resolution high-image-quality image display.

While the present invention has been described with respect to what presently are considered to be the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, the present invention is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

Claims

1. A semiconductor device comprising an insulation layer, a thin-film Si layer formed on said insulation layer and having at least one monocrystal Si region therein, and an NMOS transistor and a PMOS transistor formed on said at least one monocrystal Si region, wherein a thickness T_{BOX} of said insulation layer on which said NMOS and PMOS transistors are formed, a voltage V_{SS} of a low-voltage power supply and a voltage V_{DD} of a high-voltage power supply to be connected to said NMOS and PMOS transistors satisfy a relationship expressed by the following equation:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

where $K_1 \cong \varepsilon_{BOX}(Q_{BN} + Q_{BP})$, $K_2 \cong 2\phi_{FN} + 2\phi_{FP} - 1.03$, ε_{BOX} is a dielectric constant of said base in-

sulation layer, Q_{BN} and Q_{BP} are bulk charges when widths of depl tion layers of aid NMOS and PMOS transistors are maximized, and ϕ_{FN} and ϕ_{FP} are p udo Fermi potentials of said NMOS and PMOS transistors.

2. A semiconductor device according to claim 1, wherein said monocrystal Si region comprises a thin film obtained by epitaxial growth on a porous Si substrate member.

3. A semiconductor device according to claim 1, wherein said monocrystal Si region comprises a thin film formed by separation by implanted oxygen.

4. A semiconductor device according to claim 1, wherein said monocrystal Si region comprises a thin film formed by recrystallizing a polycrystalline or amorphous Si thin film by laser annealing.

5. A liquid crystal display having a peripheral drive circuit in which a PMOS switching transistor is used as a pixel electrode switching device and a CMOS inverter is used in said peripheral drive circuit, said liquid crystal display comprising a semiconductor device, said semiconductor device comprising an insulation layer, a thin-film Si layer formed on said insulation layer and having at least one monocrystal Si region therein, and an NMOS transistor and a PMOS transistor formed on said at least one monocrystal Si region to form said CMOS inverter, wherein a thickness T_{BOX} of said insulation layer on which said NMOS and PMOS transistors are formed, a voltage V_{SS} of a low-voltage power supply and a voltage V_{DD} of a high-voltage power supply to be connected to said NMOS and PMOS transistors satisfy a relationship expressed by the following equation:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

where $K_1 \cong \varepsilon_{BOX}(Q_{BN} + Q_{BP})$, $K_2 \cong 2\phi_{FN} + 2\phi_{FP} - 1.03$, ε_{BOX} is a dielectric constant of said base insulation layer, Q_{BN} and Q_{BP} are bulk charges when widths of depletion layers of said NMOS and PMOS transistors are maximized, and ϕ_{FN} and ϕ_{FP} are pseudo Fermi potentials of said NMOS and PMOS transistors, said PMOS switching transistor being formed on a first portion of said insulation layer and said COMS inverter being formed on a second portion of said insulation layer, a thickness of said first portion being smaller than a thickness of said second portion.

FIG. 1(a)

FIG. 1(b)
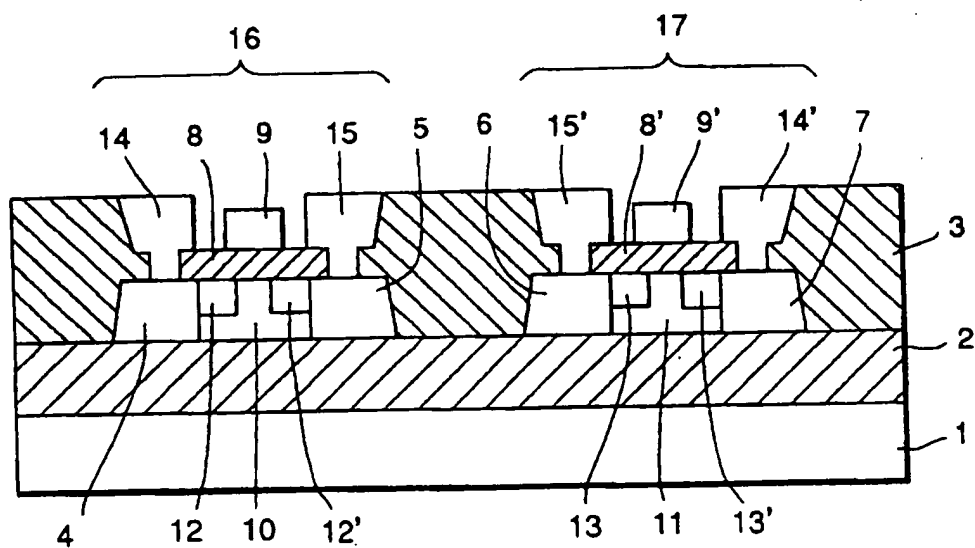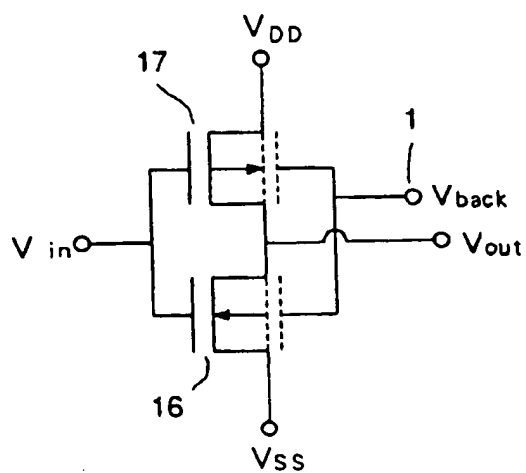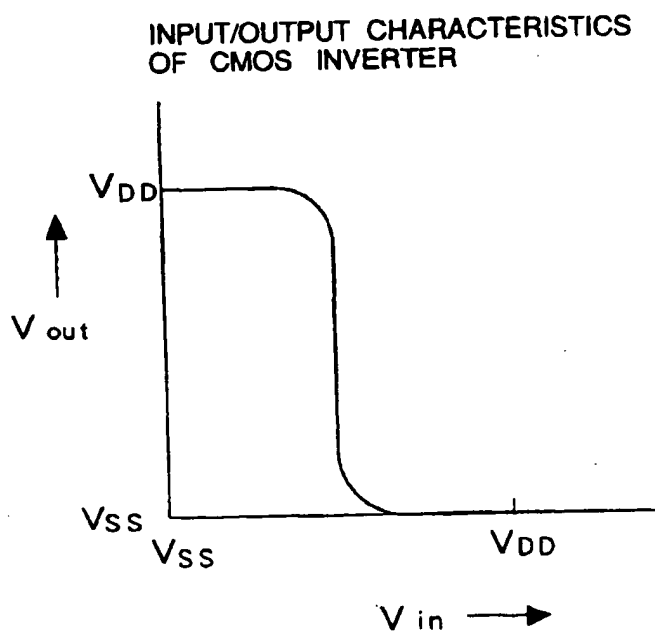
FIG. 2

INPUT/OUTPUT CHARACTERISTICS
OF CMOS INVERTER

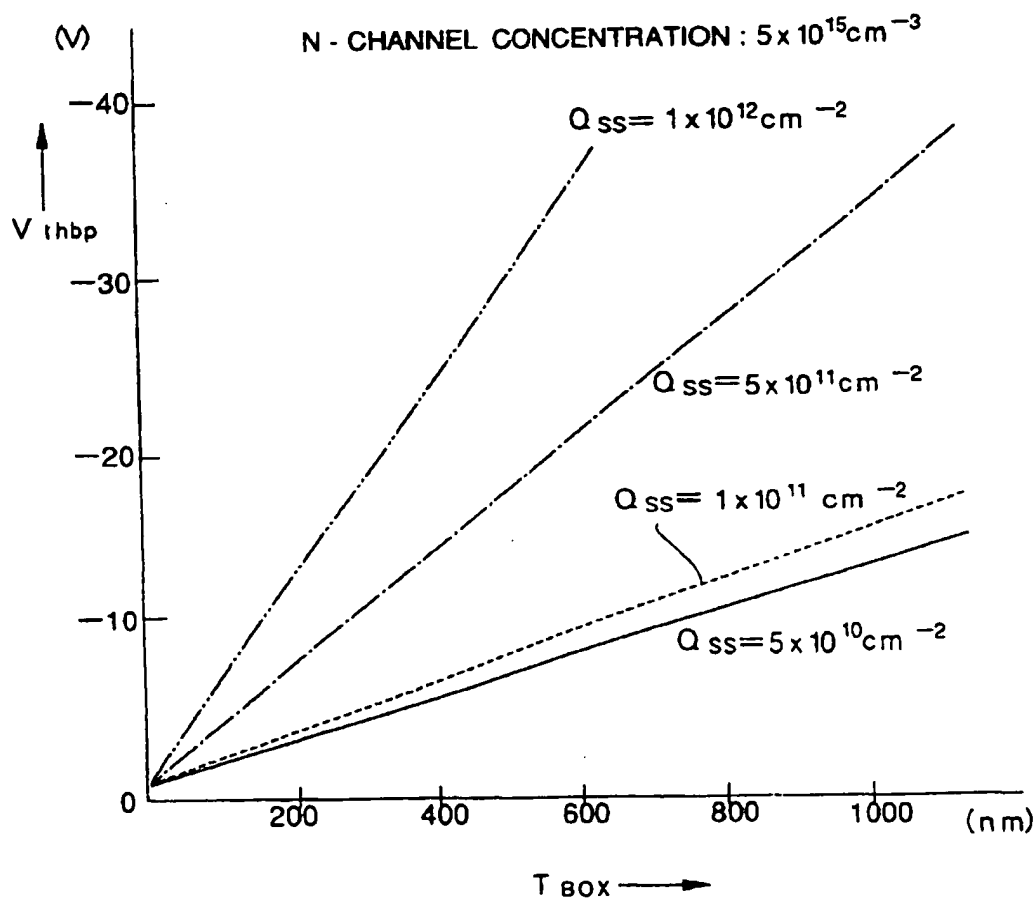# FIG. 3

FILM THICKNESS-THRESHOLD VALUE
CHARACTERISTICS OF PARASITIC NMOS
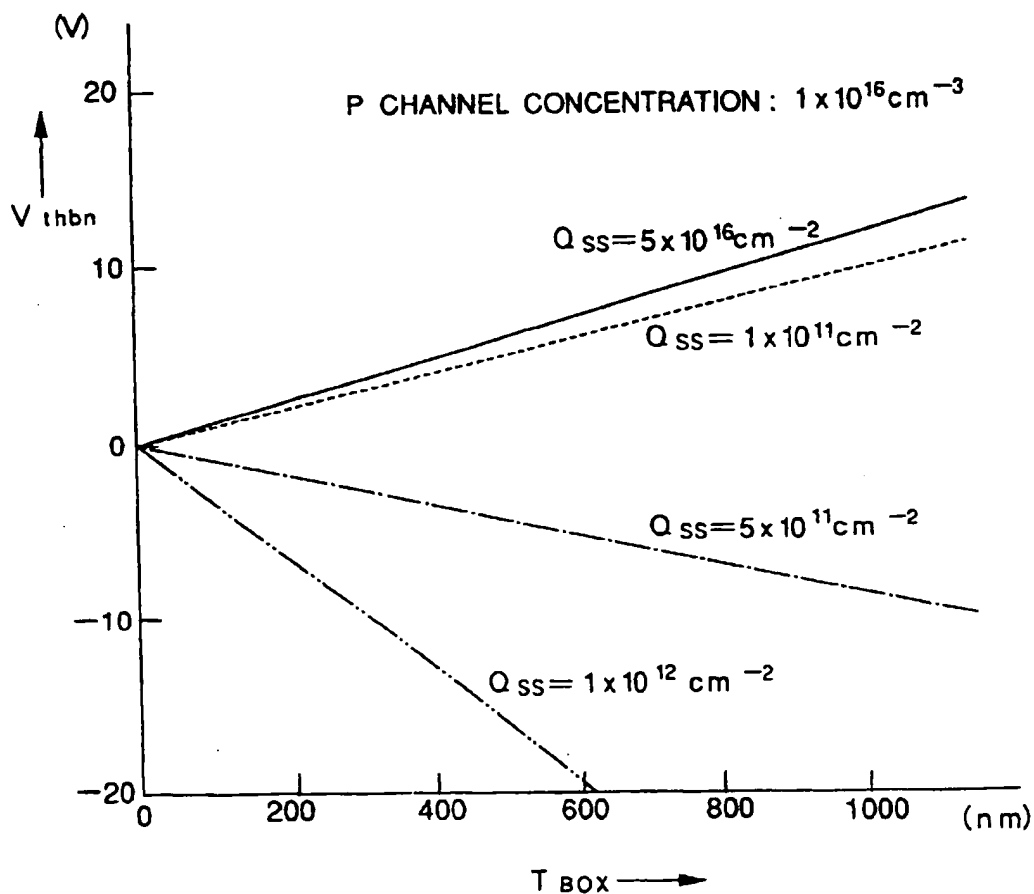
FIG. 4

FILM - THICKNESS - THRESHOLD VALUE
CHARACTERISTICS OF PARASITIC PMOS

N - CHANNEL CONCENTRATION : $5 \times 10^{15} cm^{-3}$

$Q_{ss} = 1 \times 10^{12} cm^{-2}$

$Q_{ss} = 5 \times 10^{11} cm^{-2}$

$Q_{ss} = 1 \times 10^{11} cm^{-2}$

$Q_{ss} = 5 \times 10^{10} cm^{-2}$

(V)

V_{thbp}

−40

−30

−20

−10

0

200   400   600   800   1000   (nm)

T_{BOX} ⟶

FIG. 5

PARASITIC CMOS SHUT-OFF
CURRENT / VOLTAGE MARGIN

NMOS CHANNEL DENSITY : $1 \times 10^{16} cm^{-3}$
PMOS CHANNEL DENSITY : $5 \times 10^{15} cm^{-3}$
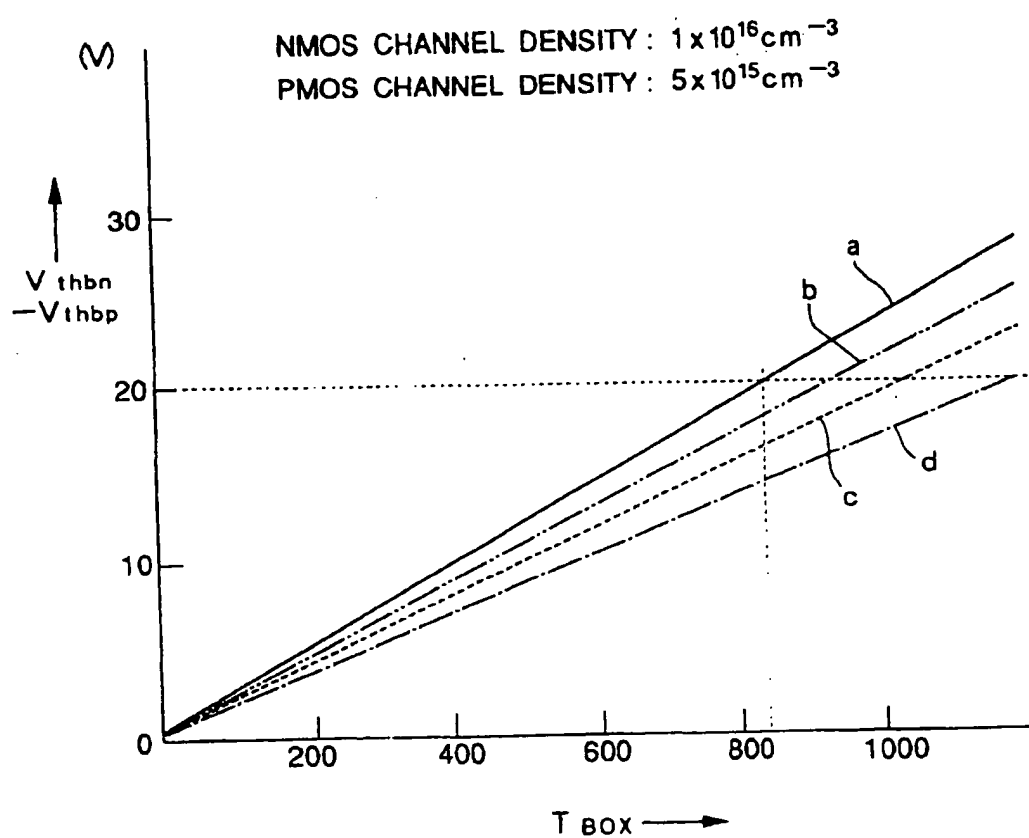
a : ALLOWABLE CURRENT 1 μA
b : ALLOWABLE CURRENT 10 μA
c : ALLOWABLE CURRENT 100 pA
d : ALLOWABLE CURRENT 1pA

FIG. 6(a)

FIG. 6(b)

FIG. 7(a)

71

72

FIG. 7(b)

76

75

74

1

73
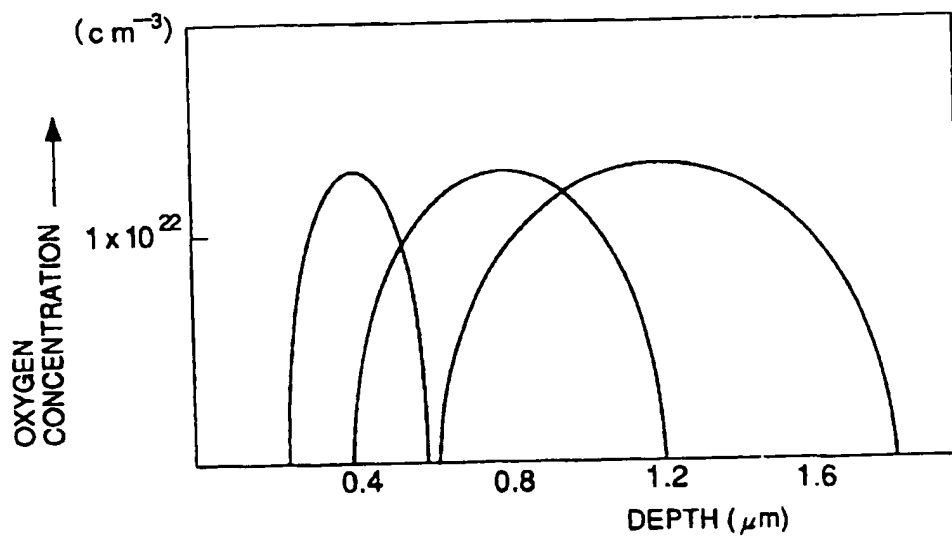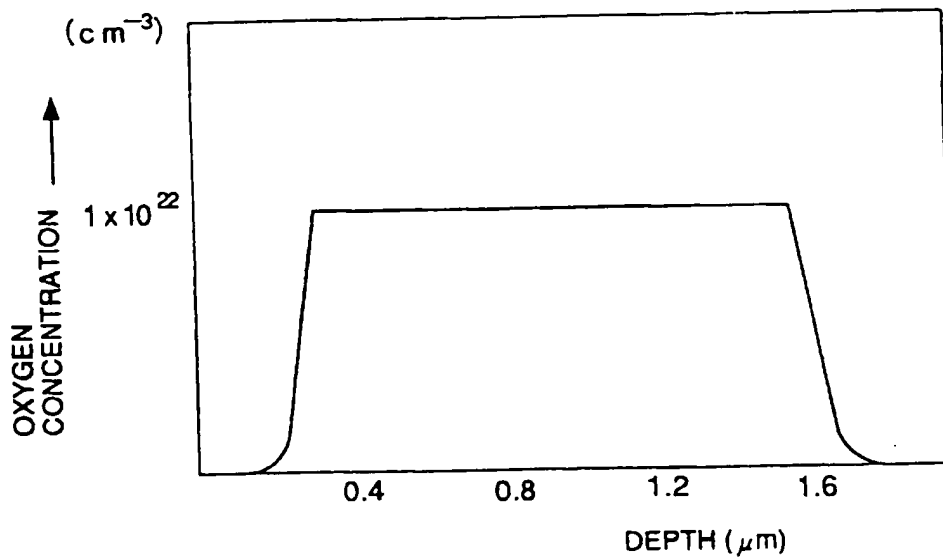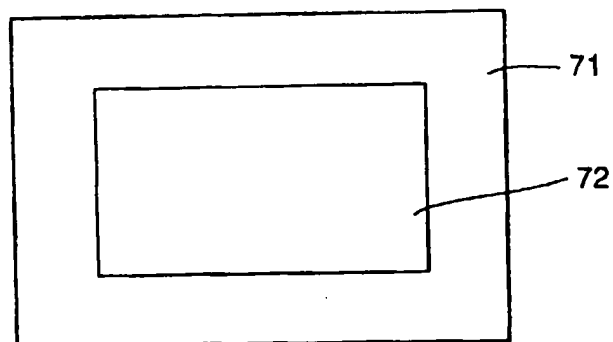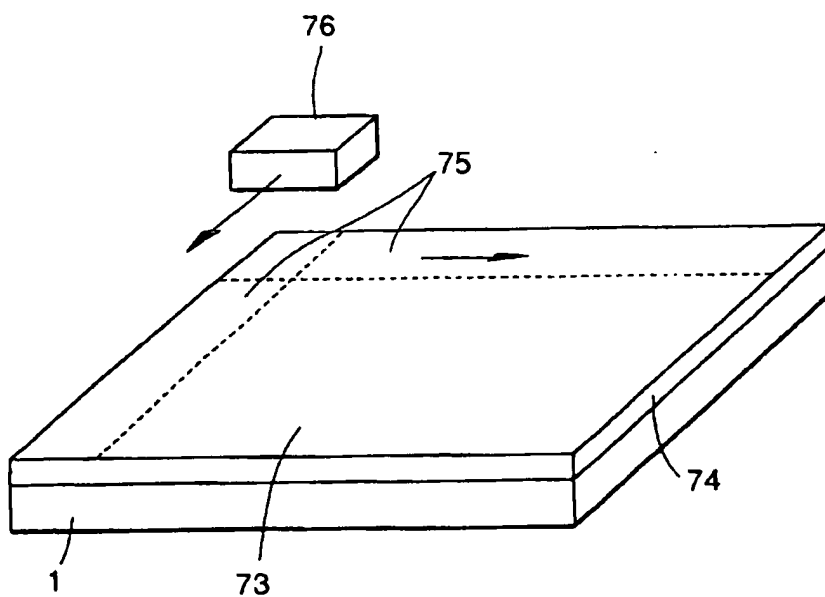
FIG. 8
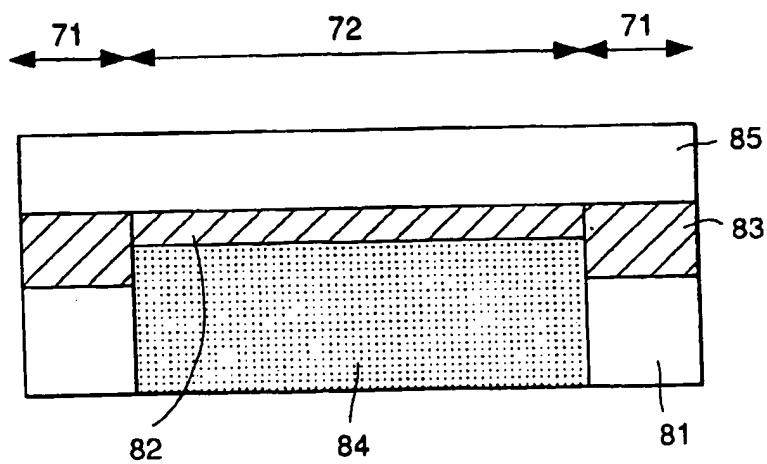
FIG. 9
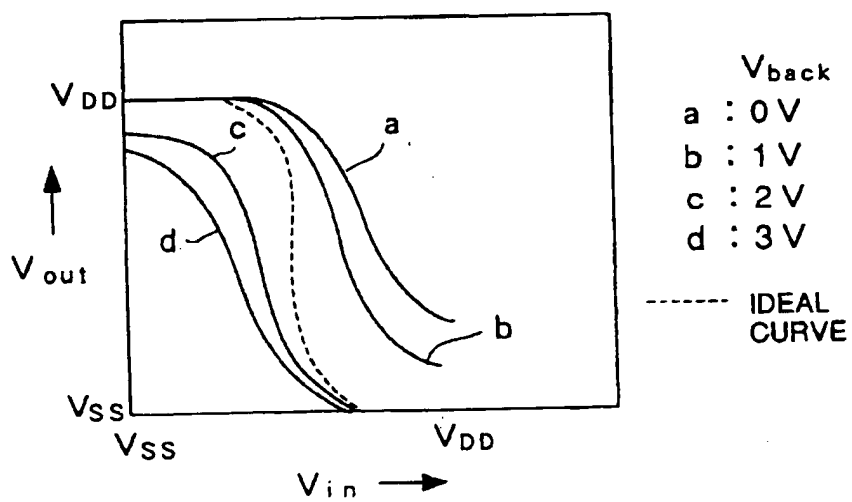
EP 0 554 063 A1

European Patent Office	EUROPEAN SEARCH REPORT	Application Number
		EP 93 30 0572

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	WO-A-8 902 095 (HUGHES AIRCRAFT COMPANY) * abstract *	1-5	H01L27/12
A	US-A-4 409 724 (TASCH, JR. ET AL.) * abstract *	1-5	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 402 (E-673)(3249) 25 October 1988 & JP-A-63 142 851 (MATSUSHITA ELECTRONICS CORP) * abstract *	1-5	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 APRIL 1993	ONSHAGE A.C.

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